Kuwait University
Computer Engineering Department
CpE 262 - Introduction to Digital Logic
Homework # 5

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1. Draw the timing diagram for the signal "Q" if the input signals are as shown below assuming the flip-flop used is a T-FF with asynchronous preset and clear signals.

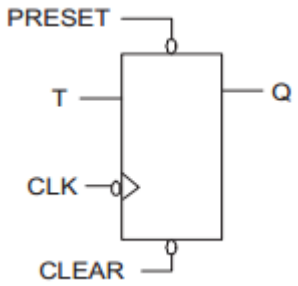

Figure 1: T-FF with Asynchronous Clear/Preset

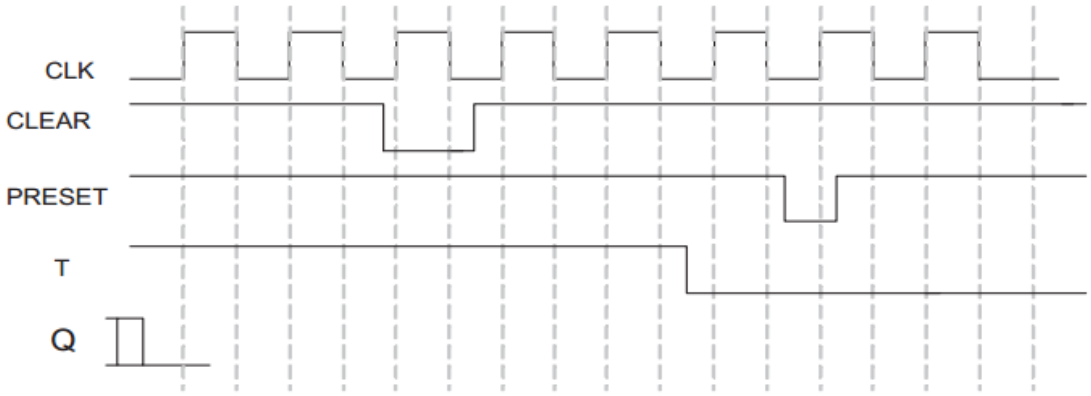

Figure 2: Timing Diagram

2. Design a JK flip-flop using a T flip-flop and other logic gates. Show all your work.

3. Show a circuit that implements the gated SR latch using NAND gates only.

4. Given a 100-MHz clock signal, drive a circuit using D flip-flop to generate 50-MHz and 25 MHz clock signals. Draw a timing diagram for all three clock signals, ignoring delays.